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NOBUHIKO MATSUMOTO residing at 725 Espellete Place, Montebello, CALIFORNIA 90640, U.S.A., declares:

(1) that he knows well both the Japanese and English languages;

(2) that he translated the Japanese patent application entitled "SEMICONDUCTOR DEVICE AND METHOD FOR MANUFACTURING THE SAME, CIRCUIT SUBSTRATE AND ELECTRONIC APPARATUS" from Japanese to English;

(3) that the attached English translation is a true and correct translation of the above-identified Japanese document to the best of his knowledge and belief; and

(4) that all statements made of his own knowledge are true and that all statements made on information and belief are believed to be true, and further that these statements are made with the knowledge that willful false statements and the like are punishable by fine or imprisonment, or both, under 18 USC 1001, and that such false statements may jeopardize the validity of the application or any patent issuing thereon.

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[List of Documents Attached]

[Name of Document]	Specification	1
[Name of Document]	Drawings	1
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[NAME OF DOCUMENT] SPECIFICATION

[TITLE OF THE INVENTION]

SEMICONDUCTOR DEVICE AND METHOD FOR MANUFACTURING THE SAME, CIRCUIT SUBSTRATE AND ELECTRONIC APPARATUS

[SCOPE OF CLAIMS]

[Claim 1] A semiconductor device comprising:

a die pad;

a plurality of semiconductor chips stacked on one surface of the die pad;

a lead extending toward the die pad;

a first wire that is bonded to a first pad of a first semiconductor chip among the plurality of semiconductor chips and to a second pad of a second semiconductor chip among the plurality of semiconductor chips;

a second wire that is bonded to the lead and to one of the first pad and the second pad; and

a sealing material that seals the plurality of semiconductor chips and exposes another surface of the die pad.

[Claim 2] A semiconductor device according to claim 1, wherein the second semiconductor chip is mounted on the first semiconductor chip, and the second wire is bonded to the lead and to the second pad.

[Claim 3] A semiconductor device according to claim 2, wherein the second wire is lead out to pass above the first wire.

[Claim 4] A semiconductor device according to claim 2 or claim 3, wherein the second wire is lead out to traverse the first wire.

[Claim 5] A semiconductor device according to any one of claim 2 through claim 4, wherein the second wire is overlapped with and bonded to the first wire on the second pad.

[Claim 6] A semiconductor device according to claim 5, wherein the second wire includes a ball formed on a tip thereof, and the ball is press-bonded to the first wire.

[Claim 7] A semiconductor device according to any one of claim 2 through claim 4, wherein the second wire is bonded to the second pad that is bonded to the first wire, while avoiding a bonded section of the first wire.

[Claim 8] A semiconductor device according to any one of claim 2 through claim 4, wherein

the second semiconductor chip includes a plurality of the second pads,

the plurality of the second pads includes a group of pads that are electrically connected to one another by a wiring,

the first wire is bonded to one of the group of pads, and

the second wire is bonded to another of the group of pads.

[Claim 9] A semiconductor device according to any one of claim 2 through claim 8, wherein

the second pad is provided with a bump, and

the first wire and the second wire are bonded to the second pad through the bump.

[Claim 10] A semiconductor device according to claim 1, wherein the second semiconductor chip is mounted on the first semiconductor chip, and the second wire is bonded to the lead and to the first pad.

[Claim 11] A semiconductor device according to any one of claim 2 through claim 10, wherein the first semiconductor chip is a memory, and the second semiconductor chip is a microprocessor.

[Claim 12] A circuit substrate that mounts the semiconductor device according to any one of claim 1 through claim 11.

[Claim 13] An electronic device that includes the semiconductor device according to any one of claim 1 through claim 11.

[Claim 14] A method for manufacturing a semiconductor device, the method comprising the steps of:

(a) stacking a plurality of semiconductor chips on one surface of a die pad;

(b) bonding a first wire to a first pad of a first semiconductor chip among the plurality of semiconductor chips and to a second pad of a second semiconductor chip among the plurality of semiconductor chips;

(c) bonding a second wire to a lead that extends toward the die pad and to one of the first pad and the second pad; and

(d) sealing the plurality of semiconductor chips and exposing another surface of the die pad.

[Claim 15] A method for manufacturing a semiconductor device according to claim 14, wherein,

in the step (a), the second semiconductor chip is mounted on the first semiconductor chip, and

in the step (c), the second wire is bonded to the lead and the second pad.

[Claim 16] A method for manufacturing a semiconductor device according to claim 15, wherein,

in the step (c), the second wire is lead out to pass over the first wire.

[Claim 17] A method for manufacturing a semiconductor device according to claim 15 or claim 16, wherein,

in the step (c), the second wire is lead out to traverse the first wire.

[Claim 18] A method for manufacturing a semiconductor device according to any one of claim 15 through claim 17, wherein,

in the step (c), the second wire is overlapped with and bonded to the first wire on the second pad.

[Claim 19] A method for manufacturing a semiconductor device according to claim 18, wherein,

in the step (c), a ball is formed on a tip portion of the second wire, and the ball is press-bonded to the first wire.

[Claim 20] A method for manufacturing a semiconductor device according to claim 18, wherein,

in the steps (b) and (c), the first wire and the second wire are bonded to the second pad without forming balls.

[Claim 21] A method for manufacturing a semiconductor device according to any one of claim 15 through claim 17, wherein,

in the step (c), the second wire is bonded to the second pad that is bonded to the first wire, while avoiding a bonded section of the first wire.

[Claim 22] A method for manufacturing a semiconductor device according to any one of claim 15 through claim 17, wherein

the second semiconductor chip includes a plurality of the second pads,

the plurality of the second pads includes a group of pads that are electrically connected to one another by a wiring,

in the step (b), the first wire is bonded to one of the group of pads, and

in the step (c), the second wire is bonded to another of the group of pads.

[Claim 23] A method for manufacturing a semiconductor device according to any one of claim 15 through claim 22, wherein,

in the step (b) and the step (c),

the second pad is provided with a bump, and

the first wire and the second wire are bonded to the second pad through the bump.

[DETAILED DESCRIPTION OF THE INVENTION]

[0001]

[TECHNICAL FIELD OF THE INVENTION]

The present invention relates to semiconductor devices, methods for manufacturing the same, circuit substrates and electronic devices.

[0002]

[CONVENTIONAL TECHNOLOGY]

Semiconductor devices having a stacked structure that realizes a high density mounting are known. For example, a known configuration includes a plurality of semiconductor chips stacked one on top of the other on a die pad of a lead frame, in which the semiconductor chips are electrically connected to leads by wires. In this case, electrodes of each of the semiconductor chips are directly bonded to the leads by the wires.

[0003]

However, the distance between the electrodes of the semiconductor chips and the leads is greater than the distance between the electrodes of the different semiconductor chips. Also, when the wires are routed around from the leads as starting points to each of the semiconductor chips, the entire length of the wires becomes long. For this reason, the resistance of the wires becomes greater, which have sometimes prevented improvements toward higher speeds. Also, since the wires are long, and therefore apt to become short-circuited with other wires.

[0004]

The present invention is provided to solve the problems described above, and its object is to improve the reliability and achieve higher speed in semiconductor devices with a stacked structure.

[0005]

[MEANS TO SOLVE THE PROBLEMS]

(1) A semiconductor device in accordance with the present invention comprises:

a die pad;

a plurality of semiconductor chips stacked on one surface of the die pad;

a lead extending toward the die pad;

a first wire that is bonded to a first pad of a first semiconductor chip among the plurality of semiconductor chips and to a second pad of a second semiconductor chip among the plurality of semiconductor chips;

a second wire that is bonded to the lead and to one of the first pad and the second pad; and

a sealing material that seals the plurality of semiconductor chips and exposes another surface of the die pad.

[0006]

In accordance with the present invention, the first wire is bonded to the first pad of the first semiconductor chip and the second pad of the second semiconductor chip. In other words, the first and second semiconductor chips are directly, electrically connected to each other by the first wire. For this reason, the entire length of the wires (the length of the first and second wires combined) can be made shorter compared to the case where wires are lead out from the leads as starting points to the first and second pads. As a result, the material cost for the wires can be reduced, and semiconductor devices can achieve higher speeds as the entire wire resistance can be lowered. Also, since the overall wire length is short, the first and second wires are prevented from becoming short-circuited.

[0007]

(2) In the semiconductor device, the second semiconductor chip may be mounted on the first semiconductor chip, and the second wire may be bonded to the lead and to the second pad.

[0008]

(3) In the semiconductor device, the second wire may be lead out to pass above the first wire.

[0009]

As a result, the first and second wires are prevented from becoming short-circuited.

[0010]

(4) In the semiconductor device, wherein the second wire may be lead out to traverse the first wire.

[0011]

As a result, the second wire can be routed around freely without being limited to configurations in which the first wire is routed around.

[0012]

(5) In the semiconductor device, the second wire may be overlapped with and bonded to the first wire on the second pad.

[0013]

As a result, even when the second pad region is narrow, a plurality of wires can be bonded to the second pad.

[0014]

(6) In the semiconductor device, the second wire may include a ball formed on a tip thereof, and the ball may be press-bonded to the first wire.

[0015]

As a result, by press-bonding the ball on the second wire to a part of the first wire on the second pad, the bonded section of the first wire and the second wire can be reinforced.

[0016]

(7) In the semiconductor device, the second wire may be bonded to the second pad that is bonded to the first wire, while avoiding a bonded section of the first wire.

[0017]

As a result, for example, the first and second wires do not have to be overlapped with each other, and therefore the first and second wires can be securely bonded to the second pad.

[0018]

(8) In the semiconductor device,

the second semiconductor chip may include a plurality of the second pads,

the plurality of the second pads may include a group of pads that are electrically connected to one another by a wiring,

the first wire may be bonded to one of the group of pads, and

the second wire may be bonded to another of the group of pads.

[0019]

As a result, for example, the first and second wires do not have to be overlapped with each other, and therefore the first and second wires can be securely bonded to the second pad.

[0020]

(9) In the semiconductor device,

the second pad may be provided with a bump, and

the first wire and the second wire may be bonded to the second pad through the bump.

[0021]

(10) In the semiconductor device, the second semiconductor chip may be mounted on the first semiconductor chip, and the second wire may be bonded to the lead and to the first pad.

[0022]

(11) In the semiconductor device, the first semiconductor chip may be a memory, and the second semiconductor chip may be a microprocessor.

[0023]

(12) A circuit substrate in accordance with the present invention mounts the aforementioned semiconductor device.

[0024]

(13) An electronic device in accordance with the present invention includes the aforementioned semiconductor device.

[0025]

(14) A method for manufacturing a semiconductor device in accordance with the present invention comprises the steps of:

(a) stacking a plurality of semiconductor chips on one surface of a die pad;

(b) bonding a first wire to a first pad of a first semiconductor chip among the plurality of semiconductor chips and to a second pad of a second semiconductor chip among the plurality of semiconductor chips;

(c) bonding a second wire to a lead that extends toward the die pad and to one of the first pad and the second pad; and

(d) sealing the plurality of semiconductor chips and exposing another surface of the die pad.

[0026]

In accordance with the present invention, the first wire is bonded to the first pad of the first semiconductor chip and the second pad of the second semiconductor chip. In other words, the first and second semiconductor chips are directly, electrically connected to each other by the first wire. For this reason, the entire length of the wires (the length of the first and second wires combined) can be made shorter compared to the case where wires are lead out

from the leads as starting points to the first and second pads. As a result, the material cost for the wires can be reduced, and semiconductor devices can achieve higher speeds as the entire wire resistance can be lowered. Also, since the overall wire length is short, the first and second wires are prevented from becoming short-circuited.

[0027]

(15) In the method for manufacturing a semiconductor device,

in the step (a), the second semiconductor chip may be mounted on the first semiconductor chip, and

in the step (c), the second wire may be bonded to the lead and the second pad.

[0028]

(16) In the method for manufacturing a semiconductor device,

in the step (c), the second wire may be lead out to pass over the first wire.

[0029]

As a result, the first and second wires are prevented from becoming short-circuited.

[0030]

(17) In the method for manufacturing a semiconductor device,

in the step (c), the second wire may be lead out to traverse the first wire.

[0031]

As a result, the second wire can be routed around freely without being limited to configurations in which the first wire is routed around.

[0032]

(18) In the method for manufacturing a semiconductor device,

in the step (c), the second wire may be overlapped with and bonded to the first wire on the second pad.

[0033]

As a result, even when the second pad region is narrow, a plurality of wires can be bonded to the second pad.

[0034]

(19) In the method for manufacturing a semiconductor device,

in the step (c), a ball may be formed on a tip portion of the second wire, and the ball may be press-bonded to the first wire.

[0035]

As a result, by press-bonding the ball on the second wire to a part of the first wire on the second pad, the bonded section of the first wire and the second wire can be reinforced.

[0036]

(20) In the method for manufacturing a semiconductor device,

in the steps (b) and (c), the first wire and the second wire may be bonded to the second pad without forming balls.

[0037]

(21) In the method for manufacturing a semiconductor device,

in the step (c), the second wire may be bonded to the second pad that is bonded to the first wire, while avoiding a bonded section of the first wire.

[0038]

As a result, for example, the first and second wires do not have to be overlapped with each other, and therefore the first and second wires can be securely bonded to the second pad.

[0039]

(22) In the method for manufacturing a semiconductor device, the second semiconductor chip may include a plurality of the second pads,

the plurality of the second pads may include a group of pads that are electrically connected to one another by a wiring,

in the step (b), the first wire may be bonded to one of the group of pads, and

in the step (c), the second wire may be bonded to another of the group of pads.

[0040]

As a result, for example, the first and second wires do not have to be overlapped with each other, and therefore the first and second wires can be securely bonded to the second pad.

[0041]

(23) In the method for manufacturing a semiconductor device,

in the step (b) and the step (c),

the second pad may be provided with a bump, and

the first wire and the second wire may be bonded to the second pad through the bump.

[0042]

[EMBODIMENT OF THE PRESENT INVENTION]

Embodiments of the present invention will be described below with reference to the accompanying drawings. However, the present invention is not limited to the embodiments to be described below.

[0043]

(First Embodiment)

Referring to Figs. 1 (A) – Fig 6 (C), a semiconductor device in accordance with a first embodiment and a method for manufacturing the same will be described.

[0044]

As shown in Fig. 1 (A), the semiconductor device in accordance with the present embodiment includes multiple semiconductor chips, a die pad 30, leads 34, first and second wires 40 and 50, and sealing material 60. Fig. 1 (B) is a

plan view in part of the semiconductor device for describing a configuration of the first and second wires 40 and 50.

[0045]

The multiple semiconductor chips include first and second semiconductor chips 10 and 20. In Fig. 1 (A), two semiconductor chips (the first and second semiconductor chips 10 and 20) are stacked in layer. Alternatively, three or more semiconductor chips can be stacked in layer. In such a case, the first and second semiconductor chips 10 and 20 correspond to two of the multiple semiconductor chips.

[0046]

The first semiconductor chip 10 may often have a rectangular solid configuration. Circuit elements (such as transistors) are formed in one of faces of the first semiconductor chip. The first semiconductor chip 10 includes one or multiple first pads 12. The first pad 12 may be a rectangular-(for example, square) shaped pad, or a circular round-shaped pad. The first pad 12 may be formed into a thin, flat configuration with aluminum metal or copper metal. The first pad 12 may often be formed on the side of the surface where circuit elements are provided. The first pad 12 may often be arranged along at least one of the sides (for example, along opposing two or four sides) of a face of the first semiconductor chip 10. Also, a passivation film (not shown) is formed on the first semiconductor chip 10 except at least one part of the first pad 12. The passivation film is formed from, for example, SiO_2, SiN, polyimide resin or the like.

[0047]

The second semiconductor chip 20 may be in a similar figure of the first semiconductor chip 10. When the second semiconductor chip 20 is mounted on the first semiconductor chip 10, the outer shape of the second semiconductor chip 20 may preferably be smaller than the outer shape of the first

semiconductor chip 10. The second semiconductor chip 20 has one or multiple second pads 22. For the other structure, the description made above for the first semiconductor chip 10 can be applied.

[0048]

The first and second semiconductor chips 10 and 20 are stacked in layer on the die pad 30. The die pad 30 is formed through processing copper or iron plate material, and generally in a rectangular configuration. In Fig. 1 (A), the first semiconductor chip 10 is mounted on the die pad 30, and the second semiconductor chip 20 is mounted on the first semiconductor chip 10. In this case, the first semiconductor chip 10 is face-up bonded to the die pad 30, and the second semiconductor chip 20 is face-up bonded to the first semiconductor chip 10. The second semiconductor chip 20 is mounted on the first semiconductor chip 10 in a manner to avoid the multiple first pads 12. The second semiconductor chip 20 may be mounted generally in the center of the first semiconductor chip 10.

[0049]

In Fig. 1 (A), the first semiconductor chip 10 is adhered to the die pad 30 by adhesive 32. The adhesive 32 may be present in a gap between the first and second semiconductor chips 10 and 20. A thermosetting resin may be used as the adhesive 32, or a material having a high heat transfer rate such as metal paste (silver paste or the like) may be used. By doing so, the heat generated during operation of the first and second semiconductor chips 10 and 20 can be readily emanated through the die pad 30.

[0050]

Multiple leads 34 extend toward the die pad 30. The leads 34 may often be formed from the same material as that of the die pad 30. The leads 34 include inner leads 36 and outer leads 38. The inner leads 36 are portions that are to be sealed by sealing material 60 (to be described later), and the outer

leads 38 are portions that are lead out the sealing material 60, and are used for electrical connection with external elements. The outer leads 38 are bent in a specified shape (a gull-wing shape in Fig. 1 (A)). Metal coating 39 of brazing material (for example, solder) or zinc may be formed on the outer leads 38.

[0051]

The first pads 12 and the second pads 22 are electrically connected to one another by first wires 40. More specifically, one end section of the first wire 40 is bonded to the first pad 12, and the other end section of the first wire 40 is bonded to the second pad 22. The first wires 40 may be formed from metal, such as, for example, gold, aluminum or copper.

[0052]

Bumps 42 may be provided on the first pads 12. The material of the bumps 42 may preferably be the same material of the first wires 40 to be bonded, and may be, for example, gold. The bumps 42 may be part of the first wires 40. In other words, the bumps 42 may be formed from balls that are formed at tip sections of the first wires 40 and squashed. By forming the bumps 42 at the first pads 12, the bonding strength between the first wires 40 and the first pads 12 can be enhanced.

[0053]

In the present embodiment, the second pads 22 and the leads 34 (more specifically, the inner leads 36) are electrically connected to one another by second wires 50. More specifically, one end section of the second wire 50 is bonded to the second pad 22, and the other end section of the second wire 50 is bonded to the lead 34. The second wires 50 may be formed from the same material as that of the first wires 40.

[0054]

Bumps 52 may be provided on the second pads 22. The material of the bumps 52 may preferably be the same material of the first and second wires 40

and 50 to be bonded, and may be, for example, gold. The bumps 52 may be part of the second wires 50. In other words, the bumps 52 may be formed from balls that are formed at tip portions of the second wires 50 and squashed. By forming the bumps 52 at the second pads 22, the bonding strength between the second wires 50 and the second pads 22 can be enhanced.

[0055]

Alternatively, the bumps 52 may be part of the first wires 40. Also, bumps may be provided on the leads 34 at their bonding sections with the second wires 50 (see Fig. 6 (C)). By forming the bumps on the leads 34, the bonding strength between the second wires 50 and the leads 34 can be enhanced.

[0056]

As shown in Fig. 1 (A), the second wires 50 are lead out above the first wires 40. In other words, loops of the first wires 40 are lead out in a manner not to exceed loops of the second wires 50. By so doing, the first and second wires 40and 50 can be prevented from becoming short-circuited.

[0057]

In the example shown in Fig. 1(A) and Fig. 1(B), the first and second wires 40 and 50 are overlapped with one another on and bonded to the second pads 22. By this, the leads 34 and the first pads 12 can be electrically connected through the first and second wires 40 and 50. Moreover, even when the second pads 22 are provided in a narrow region, the first and second wires 40 and 50 can be bonded to the second pads 22. The second wires 50 may be overlapped on the first wires 40. By so doing, the second wires 50 can be readily lead out above the first wires 40.

[0058]

As shown in Fig. 1 (A), the sealing material 60 seals the multiple semiconductor chips. More specifically, the sealing material 60 seals the first

and second semiconductor chips 10 and 20, the first and second wires 40 and 50, and the inner leads 36. The sealing material 60 may often be resin (for example, epoxy resin). The sealing material 60 exposes part of the die pad 30. More specifically, the sealing material 60 exposes a surface of the die pad 30 opposite to its surface where the first and second semiconductor chips 10 and 20 are mounted. By so doing, the heat generated during operation of the first and second semiconductor chips 10 and 20 can be readily emanated through the die pad 30.

[0059]

As shown in Fig. 2, the second wire 50 may be lead out in a manner to traverse the first wire 40. More specifically, in a plan view of the first and second semiconductor chips 10 and 20, the first and second wires 40 and 50 may cross each other. In this case, the first and second wires 40 and 50 are disposed in a manner not to contact with each other. For example, the second wire 50 may be lead out above the first wire 40. By this, the second wire 50 can be routed around freely without being restricted by the configuration in which the first wire 40 is routed. In other words, the positions of the first pads 12, second pads 22 and leads 34 can be freely designed without being limited by the configuration in which the first and second wires 40 and 50 are routed.

[0060]

The multiple semiconductor chips may include, for example, a variety of memories such as a flash memory, SRAM (Static RAM) and DRAM (Dynamic RAMs), or a microprocessor such as MPU (Micro Processor Unit) and MCU (Micro Controller Unit). For example, the first and second semiconductor chips 10 and 20 may be a combination of a memory and a microprocessor, or memories (a flash memory and an SRAM, SRAMs, or DRAMs). In the example shown in Fig. 1 (A), the first semiconductor chip 10 is a memory (for example, a flash memory), and the second semiconductor chip 20 is a microprocessor.

[0061]

Fig. 3 shows a variation example of the semiconductor device in accordance with the present embodiment. In the present variation example, the second semiconductor chip 20 includes one or multiple (one in Fig. 3) second pads 24. The first and second wires 40 and 50 are bonded to the second pad 24 in a manner that they do not overlap with each other. More specifically, the first wire 40 is bonded to part of the second pad 24, and the second wire 50 is bonded to another part of the second pad 24 at a location that avoids the bonding section of the first wire 40. In other words, in a plan view of one of the second pads 24, the bonding sections of the first and second wires 40 and 50 are arranged side by side. By this, the first and second wires 40 and 50 do not need to be overlapped with each other, such that the first and second wires 40 and 50 can be securely bonded to the second pads 24. As shown in Fig. 3, the second pad 24 may have an outer shape with an area greater than an outer shape of each of the other pads formed on the second semiconductor chip 20. For example, the second pad 24 may be a rectangle with a shorter side equivalent to one side of a square shape of each of the other pads.

[0062]

Fig. 4 shows another variation example of the semiconductor device in accordance with the present embodiment. In the present variation example, the second semiconductor chip 20 includes a group of (two in Fig. 4) pads 26 that are electrically connected by a wiring 28. The first wire 40 is bonded to one of the group of pads 26, and the second wire 50 is bonded to another one of the group of pads 26. By this, the first and second wires 40 and 50 do not have to be overlapped with each other, and therefore the first and second wires 40 and 50 can be securely bonded to the second pads 22.

[0063]

The wiring 28 is formed on a face of the second semiconductor chip 20 where the group of pads 26 are formed. The wiring 28 may be formed together with the group of pads 26 in the process of manufacturing the second semiconductor chip 20. In this case, the wiring 28 may be formed form the same material (for example, aluminum metal or copper metal) as that of the group of pads 26. As shown in Fig. 4, another pad (for example, the second pad 22) may be formed between the pads in the group of pads 26. In the present variation example, since the pads are electrically connected to one another, wires do not have to be lead out from all of the corresponding pads 26 in the group to the first semiconductor chip 10 and to the lead 34. Therefore, the number of the entire wires can be reduced.

[0064]

In accordance with the present embodiment, the first wires 40 are bonded to the first pads 12 of the first semiconductor chip 10 and to the second pads 22 of the second semiconductor chip 20. In other words, the first wires 40 are bonded to the first pads 12 of the first semiconductor chip 10 and to the second pads 22 of the second semiconductor chip 20. In other words, the first and second semiconductor chips 10 and 20 are directly, electrically connected to one another by the first wires 40. For this reason, the entire length of the wires (the length of the first and second wires 40 and 50 combined) can be made shorter compared to the case where wires are lead out from the leads 34 as starting points to the first and second pads 12 and 22. As a result, the material cost for the wires can be reduced, and semiconductor devices can achieve higher speeds as the entire wire resistance can be lowered. Also, since the overall wire length is short, the first and second wires 40 and 50 are prevented from becoming short-circuited.

[0065]

Next, descriptions will be made as to a method for manufacturing semiconductor devices in accordance with an embodiment of the present invention. Figs. 5 (A) through 6 (C) show portions of the method for manufacturing semiconductor devices (wire bonding process).

[0066]

First, a die bonding process is conducted. More specifically, first and second semiconductor chips 10 and 20 are mounted on a die pad 30. For example, by using adhesive 32, the die pad 30 and the first semiconductor chip 10 may be adhered, and the first semiconductor chip 10 and the second semiconductor chip 20 may be adhered.

[0067]

Next, a wire bonding process is conducted. For example, first pads 12 and second pads 22 are electrically connected by wires, and the second pads 22 and inner leads 36 of leads 22 are electrically connected by wires. In the wire bonding process, as indicated in the figures, a nail head method may be employed. Alternatively, a wedge method, which does not form balls at tip portions, may be employed.

[0068]

As indicated in Fig. 5 (A), a capillary 70 is disposed on the side of a face of the first semiconductor chip 10 where the first pads 12 are formed. A first wire 40 (which is a conductive line that becomes a first wire) is passed through the capillary 70. A ball 41 is formed on the first wire 40 outside the capillary 70. The ball 41 may be formed at a tip of the first wire 41 by, for example, a high voltage electrical discharge by an electric torch. Then, a clamper 72 is released to lower the capillary 70, thereby pressing the ball 41 against the first pad 12. While the ball 41 is pressed against the first pad 12 under a constant pressure to perform a contact bonding, ultrasonic or heat is applied. As a

result, the bump 42 is formed on the first pad 12, and the first wire 40 is bonded to the first pad 12 (i.e., first bonding).

[0069]

Then, the clamper 72 is closed to retain the first wire 40, and the capillary 70 and the clamper 72 are simultaneously controlled, as indicated in Fig. 5 (A), to make a loop on the first wire 40. Then, a part of the first wire 40 is pressed against the second pad 22 to perform a contact bonding with the second pad 22, thereby bonding the first wire 40 to the second pad 22 (i.e., second bonding). In other words, the first wire 40 is bonded to the second pad 22 without forming a ball. For example, when the diameter of the first wire 40 is about 25 – 30μm, a pressure of about 0.20 – 0.30N is applied to squash the first wire 40 to have a width equivalent to about 1.5 – 2 times the diameter. In this case, ultrasonic or heat is applied when performing the contact bonding.

[0070]

As indicated in Fig. 5 (A), when the position of the first bonding (for example, the position of the first pad 12) is lower than the position of the second bonding (for example, the position of the second pad 22), the loop height of the first wire 40 can be made lower, compared to the case when they are in an inverse relation. Accordingly, the semiconductor device can be made thinner.

[0071]

Next, as indicated in Fig. 5 (B), the second wire 50 is bonded to the second pad 22 and to the lead 34, in a similar manner as the bonding of the first wire 40. For example, a first bonding to the second pad 22 may be conducted, and a second bonding to the inner lead 36 may be conducted. In the first bonding, a ball 51 is formed on a tip portion of the second wire 50 in a manner described above, and the ball 51 is pressed against the second pad 22. When the first and second wires 40 and 50 are overlapped with each other and

bonded, the ball 51 is pressed against a part of the first wire 40 on the second pad 22 to form a pump 52 on the first wire 40. By so doing, the bonded section of the first wire 40 and the second pad 22 can be enforced. When the position of the first bonding (for example, the position of the second pad 22) is lower than the position of the second bonding (for example, the position of the inner lead 36), the loop height of the second wire 50 can be made lower, compared to the case when they are in an inverse relation. Accordingly, the semiconductor device can be made thinner. On the second pad 22, the first wire 40 does not form a standing portion that may rise from the bump 42. Therefore, even when the second wire 50 may be bonded on the first wire 40, the first wire 40 falls and can be prevented from becoming short-circuited with other wires.

[0072]

As a variation example of the wire bonding process, as shown in Figs. 6 (A) – 6 (C), bumps 80 may be provided on the second pads 22, and a second bonding of the second wires 50 through the bumps 80 may be conducted. The bumps 80 may preferably be formed from the same material as that of the first wires 40, and may be, for example, gold. The bump 80 may be formed as follows. A ball is formed at a tip portion of a wire (not shown), the wire is torn off at a section near its tip portion to leave the ball on the second pad 22. Then, the bump 80 may be subject to a leveling to planarize its upper surface.

[0073]

Alternatively, the bumps 80 may be formed by an electrolytic plating or an electroless plating. In this case, in the state of a semiconductor wafer, the bumps 80 may be formed all together. A surface layer of the bump 80 may preferably be formed from the same material as that of the first wire 40 (for example, gold). When the bumps 80 are formed by an electrolytic plating or an electroless plating, upper surfaces of the bumps 80 can be readily be planarized, such that the first wires 40 can be securely bonded to the bumps 80. Also, the

second pads 22 are covered by the bumps (for example, gold bumps) 80; therefore, even when the bonding position of the first wires (for example, gold wires) is somewhat shifted, they can be pressure-welded.

[0074]

As indicated in Fig. 6 (B), the second wires 50 may be bonded to the inner leads 36 in a first bonding, and to the second pads 22 in a second bonding. When the first and second wires 40 and 50 are overlapped with each other and bonded, the first and second wires 40 and 50 are bonded on the bump 80. In this case, as indicated in Fig. 6 (C), the first and second wires 40 and 50 may be bonded to the bump 80 without forming any ball.

[0075]

It is noted that the wire bonding process is not limited to the examples described above, and is applicable to all structures which may be implied by the above-description.

[0076]

After the wire bonding process is completed, a molding process is conducted. More particularly, the die pad 30 on which the first and second semiconductor chips 10 and 20 are mounted is set on a metal mold (not shown) for molding. The metal mold is composed of an upper mold and a lower mold. A recessed section is formed in each of the upper mold and the lower mold, wherein the recessed sections of both of the molds define a mold cavity. Sealing material (for example, thermosetting resin) is injected in the cavity to seal the first and second semiconductor chips 10 and 20, the first and second wires 40 and 50 and the inner leads 34.

[0077]

Thereafter, a trimming process such as cutting bump burrs, a plating process such as plating on the outer leads, a forming process and the like are conducted. Furthermore, other processes including a marking process and a

testing process are conducted. Through the processes described above, the semiconductor device is manufactured.

[0078]

The semiconductor device in accordance with the present embodiment include structures that may derive from the manufacturing method described above. The same effects described above can be obtained from the method for manufacturing semiconductor devices.

[0079]

(Second Embodiment)

Fig. 7 indicates a semiconductor device in accordance with a second embodiment of the present invention. In the present embodiment, first pads 12 and leads 34 (more specifically, inner leads 36) are electrically connected to one another by second wires 150. More specifically, one end section of the second wire 150 is bonded to the first pad 12, and the other end section of the second wire 150 is bonded to the lead 34. In this case, bumps 152 may be provided on the first pads 12, and the bumps 152 may be formed by squashed balls that are formed at tip portions of the second wires 150.

[0080]

In accordance with the present embodiment, the first and second wires 40 and 150 do not overlap with one another except at the first pads 12 when viewed in a plan view of the first semiconductor chip 40. Therefore, the first and second wires 40 and 150 can be prevented from becoming short-circuited.

[0081]

As indicated in Fig. 7, the first and second wires 40 and 150 may be overlapped and bonded to the first pad 12. In this case, the second wire 150 may be overlapped on the first wire 40, or the first wire 40 may be overlapped on the second wire 150.

[0082]

It is noted that, in the semiconductor device and its manufacturing method, the contents described in the first embodiment are applicable to the other structures and effects.

[0083]

Fig. 8 indicates a semiconductor device in accordance with a third embodiment of the present invention. In the present embodiment, three semiconductor chips 200, 210 and 220 are stacked in layer on a die pad 30. In this case, the first and second semiconductor chips described in the aforementioned embodiments correspond to two of the three semiconductor chips 200, 210 and 220.

[0084]

In Fig. 8, pads on the semiconductor chip 220 in the uppermost layer and leads 34 are electrically connected to one another by wires 230. Also, the pads on the semiconductor chip 220 in the uppermost layer and pads on the semiconductor chip 210 in the intermediate layer are electrically connected to one another by wires 232. In this case, the semiconductor chip 210 in the intermediate layer may be defined as a first semiconductor chip, the semiconductor chip 220 in the uppermost layer as a second semiconductor chip, the wires 232 as first wires, and the wires 230 as second wires, and the contents explained in the embodiments described above can be applied as much as possible. It is noted that the pads on the semiconductor chip 210 in the intermediate layer and pads on the semiconductor chip 200 in the lowermost layer are electrically connected to one another by wires 234.

[0085]

Fig. 9 shows a circuit substrate on which a semiconductor device in accordance with the present invention is mounted. An organic substrate, such as, for example, a glass epoxy substrate can be generally used as a circuit substrate 1000. Wiring patterns 1100 composed of, for example, copper or the

like are formed into a desired circuit on the circuit substrate 1000. The wiring patterns 1100 and outer leads 38 of the semiconductor device 1 are bonded to one another. Also, a heat radiation member (heat spreader) 1200 is provided on the circuit substrate 1000, wherein the heat radiation member 1200 is bonded to an exposed surface of the semiconductor device 1. By so doing, heat generated in the first and second semiconductor chips 10 and 20 can be emanated, through the die pad 30, from the heat radiating member 1200.

[0086]

Fig. 10 shows a notebook type personal computer 2000, and Fig. 11 shows a mobile telephone 3000, as electronic apparatuses that include semiconductor devices to which the present invention is applied.

[0087]

The present invention is not limited to the embodiments described above, and many modification can be made. For example, the present invention may include compositions that are substantially the same as the compositions described in the embodiments (for example, a composition that has the same functions, the same methods and the results, or a composition that have the same objects and results). Also, the present invention includes compositions in which portions not essential in the compositions described in the embodiments are replaced with others. Also, the present invention includes compositions that achieve the same functions and effects or achieve the same objects of those of the compositions described in the embodiments. Furthermore, the present invention includes compositions that include publicly known technology added to the compositions described in the embodiments.

[BRIEF DESCRIPTION OF THE DRAWINGS]

[Fig. 1]

Figs. 1 (A) and 1 (B) show a semiconductor device in accordance with a first embodiment of the present invention.

[Fig. 2]

Fig. 2 shows a semiconductor device in accordance with the first embodiment of the present invention.

[Fig. 3]

Fig. 3 shows a semiconductor device in accordance with a variation example of the first embodiment.

[Fig. 4]

Fig. 4 shows a semiconductor device in accordance with a variation example of the first embodiment.

[Fig. 5]

Figs. 5 (A) – 5 (C) show a method for manufacturing semiconductor devices in accordance with the first embodiment.

[Fig. 6]

Figs. 6 (A) – 6 (C) show a method for manufacturing semiconductor devices in accordance with a variation example of the first embodiment.

[Fig. 7]

Fig. 7 shows a semiconductor device in accordance with a second embodiment of the present invention.

[Fig. 8]

Fig. 8 shows a semiconductor device in accordance with a third embodiment of the present invention.

[Fig. 9]

Fig. 9 shows a circuit substrate on which a semiconductor device in accordance with an embodiment of the present invention is mounted.

[Fig. 10]

Fig. 10 shows an electronic apparatus in accordance with an embodiment of the present invention.

[Fig. 11]

Fig. 11 shows an electronic apparatus in accordance with an embodiment of the present invention.

[DESCRIPTION OF REFERENCE NUMBERS]

10	First semiconductor chip
12	First pad
20	Second semiconductor chip
22	Second pad
24	Second pad
26	Group of pads
30	Die pad
34	Leads
40	First wire
41	Ball
42	Bump
50	Second wire
51	Ball
52	Bump
60	Sealing material
150	Second wire
200	Semiconductor chip
210	Semiconductor chip
220	Semiconductor chip
230	Wire
232	Wire

234 Wire

[NAME OF DOCUMENT] ABSTRACT

[ABSTRACT]

[OBJECTS]

To improve the reliability and achieve higher speeds in semiconductor devices with a stacked structure.

[MEANS FOR SOLUTION]

A semiconductor device includes a die pad 30, a plurality of semiconductor chips stacked on one surface of the die pad 30, leads extending toward the die pad 30, first wires 40 that are bonded to first pads 12 of a first semiconductor chip 10 among the plurality of semiconductor chips and to second pads 22 of a second semiconductor chip 20 among the plurality of semiconductor chips, second wires 50 that are bonded to the leads and to the first pads or the second pads, and a sealing material 60 that seals the plurality of semiconductor chips and exposes another surface of the die pad 30.

[SELECTED FIGURE] Fig. 1

Fig. 1 (A)

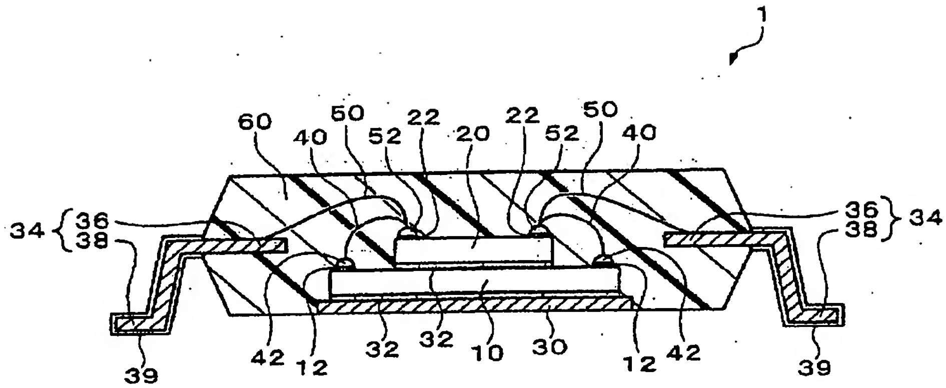
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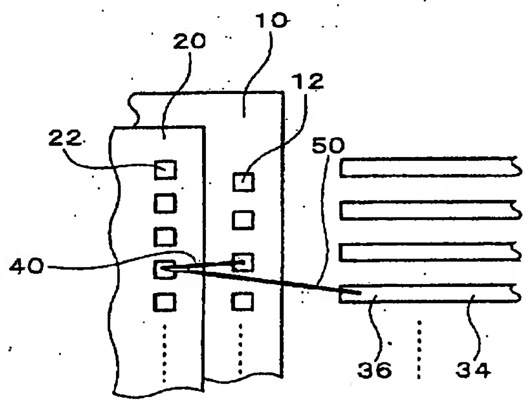
Fig. 1 (B)


10
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36
34

Fig. 2

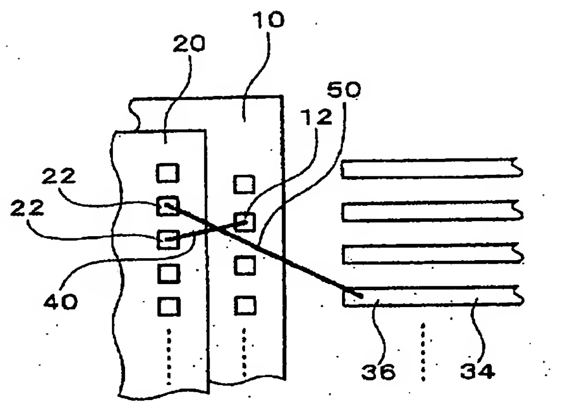

Fig. 3

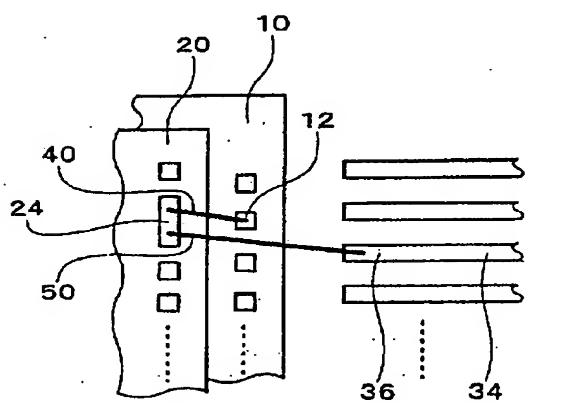

Fig. 4

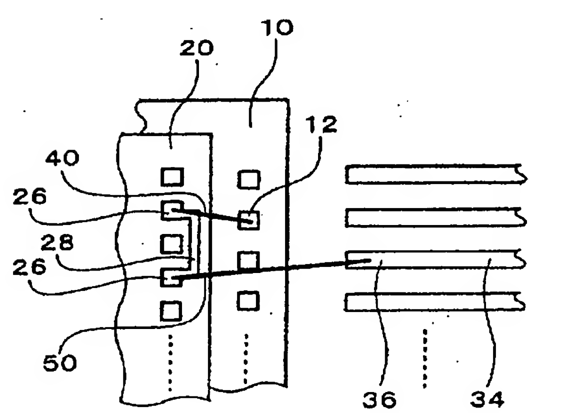

Fig. 5 (A)

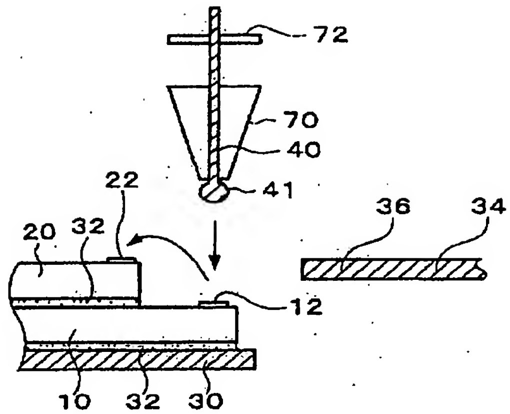

Fig. 5 (B)

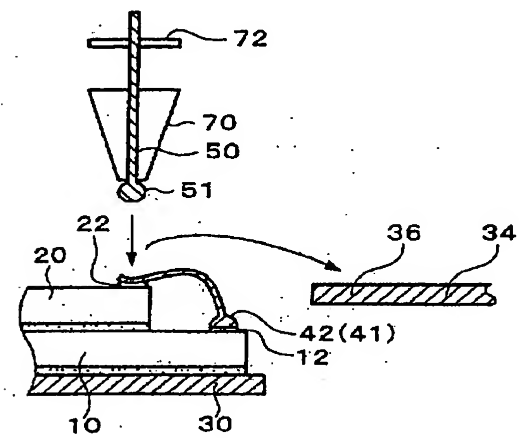

Fig. 5 (C)

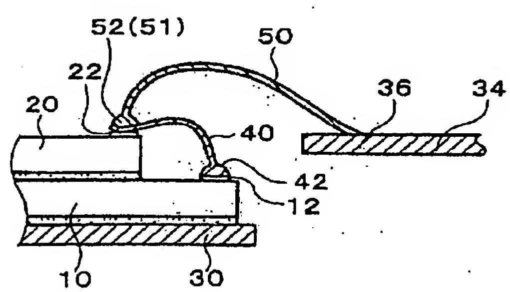

Fig. 6 (A)

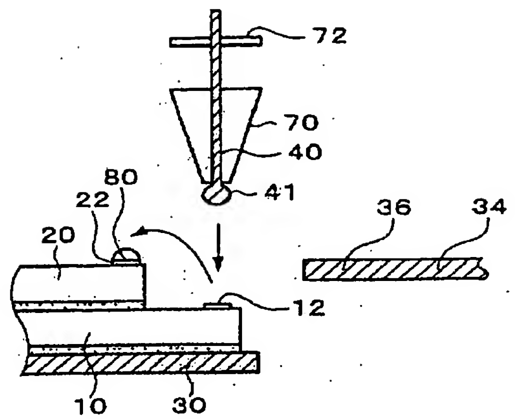

Fig. 6 (B)

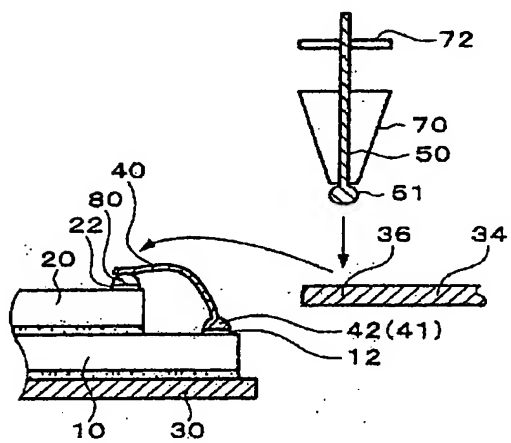

Fig. 6 (C)

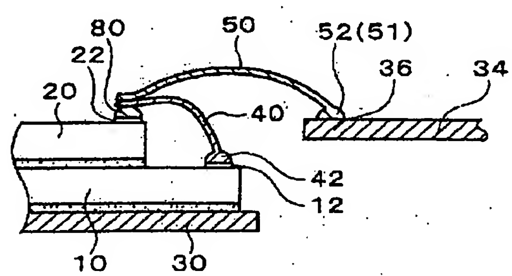

Fig. 7

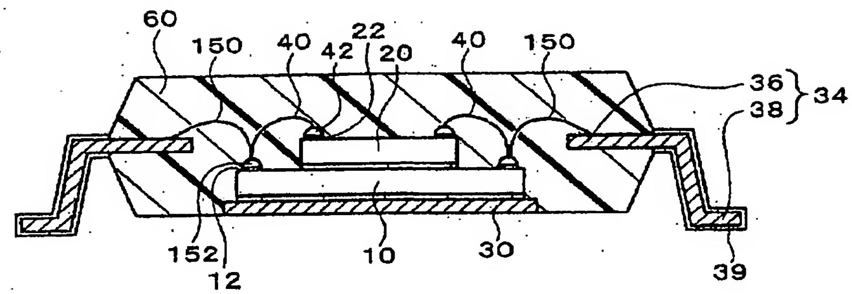

Fig. 8

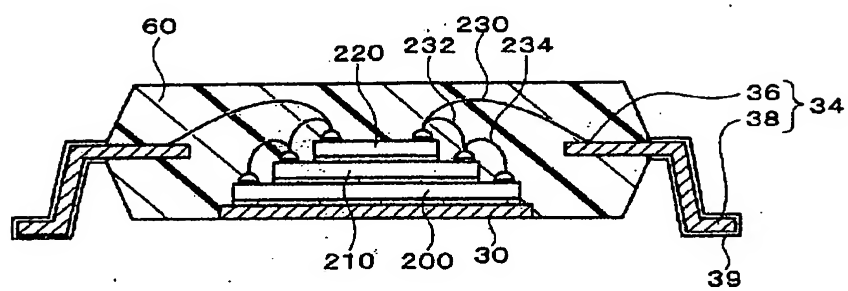

Fig. 9

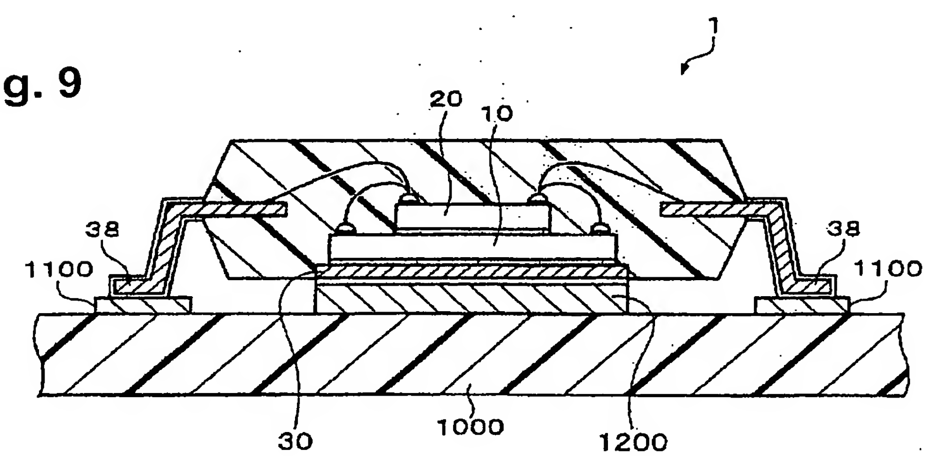

Fig. 10

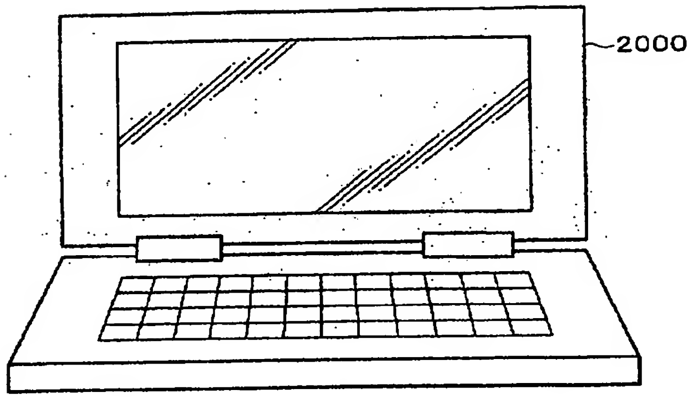

Fig. 11